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(54) Row redundancy circuit for a semiconductor memory device

(57) A row redundancy circuit for repairing a defective cell of a memory cell array in a semiconductor memory device comprises an address selector (300) for receiving three address bits designating the defective cell to selectively output one of the three address bits. A fuse box (100) stores the information of the remaining address bits except the selected bit output by the address selector, and at least one redundant decoder (200, 200A) decodes the output signals of the address selector and fuse box.

By this means it is possible to replace pairs of adjacent faulty (eg: shorted) word lines where the addresses of the two lines differ in the first, second and/or third least significant bit positions.

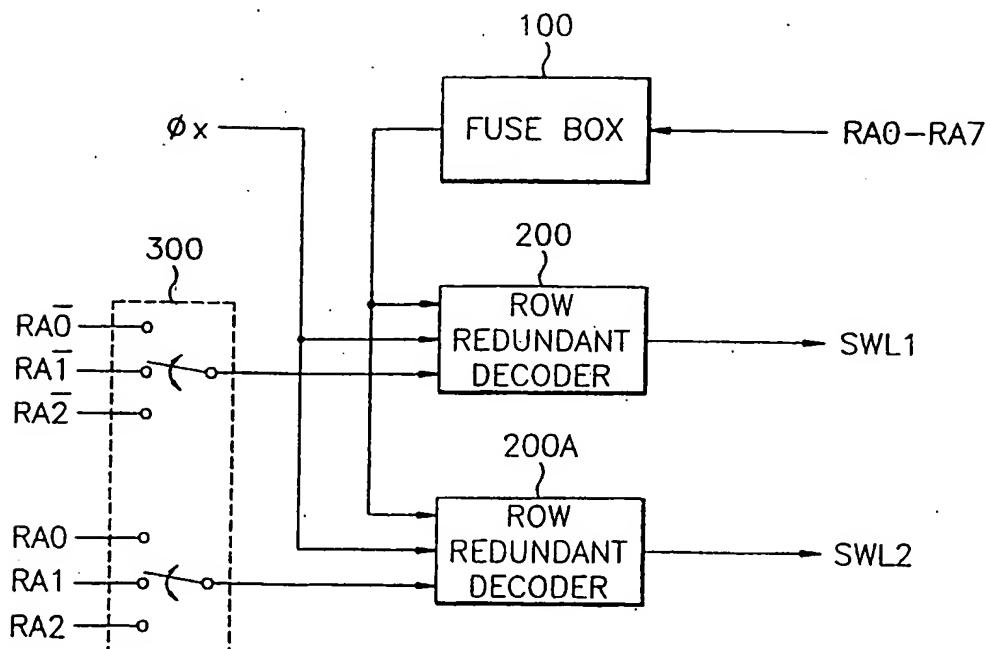


FIG. 2

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ROW REDUNDANCY CIRCUIT FOR A
SEMICONDUCTOR MEMORY DEVICE

The present invention relates to semiconductor memory devices, and
5 more particularly to a row redundancy circuit for replacing a defective cell
present in a row of a normal memory cell array with a spare cell.

Generally, a semiconductor memory device is provided with a row
redundancy circuit to replace a defective memory cell of a normal memory
10 cell array with a spare cell by decoding the row address designating the
defective cell. The spare or redundant cell array comprising the spare or
redundant memory cells is arranged adjacent to the normal cell array along
with decoders for decoding the addresses and selecting the redundant cells.

15 Each of the minimum array blocks with corresponding sense amplifier
groups is usually provided with the respective spare cell array. The number
of the minimum array blocks in a single chip tends to be increased as the
complexity of the chip increases so as to prevent the operating current drop
which is caused by the reduction of the activation of the array. Most of the
20 word line fails are usually caused by so-called cross fail such as a bridge
between two adjacent word lines. In order to cope with such cross fail, the
row redundancy circuit employs a row redundancy set comprising two word
lines so as to simultaneously repair the two failing word lines. The two
adjacent word lines are defined by the least significant bit (LSB) of the row
25 address as the internal signal. The repairing operation is usually accomplished
by storing the information of the remaining bits except LSB into a fuse box.

A conventional row redundancy circuit is shown in a block diagram of Figure 1 of the accompanying diagrammatic drawings. The output signals of row redundant decoders 200 and 200A are respectively connected to spare word lines SWL1 and SWL2. A signal ϕX is applied to the row redundant decoders 200 and 200A. Row address signals RA1-RA7 except the LSB RA0 are all transferred to the fuse box 100. The row address signals RA0 and RA $\bar{0}$ as LSBs control the row redundant decoders 200 and 200A so as to cut the fuse of the fuse box 100 by using only the information of RA1-RA7 among the row address bits designating the defective memory cell.

10

Thus, the repairing is possible only when the two adjacent word lines have the same RA1-RA7 and different RA0, so that the repairing probability is only 50%. For example, when there is provided a row redundancy set for each of the minimum array blocks, it is impossible to repair two adjacent word lines pair when a failing occurs between two adjacent word lines pairs divided by LSB. Hence this causes a reduction of the repairing probability to 50% as well as lower yield of the chips. If there are provided at least two row redundancy sets for each of the minimum array blocks in order to resolve the above problem, the chip areas occupied by the redundant cells and thus 15
20 the chip size are considerably increased.

Preferred embodiments of the present invention aim to provide a row redundancy circuit for maximizing the repairing probability of a chip.

25

It is another aim to provide a row redundancy circuit, whereby the chip repairing probability is considerably increased even with a single row redundancy set for each of the minimum array blocks in the chip.

According to one aspect of the present invention, there is provided a semiconductor memory device with a row redundancy circuit for repairing a defective cell of a memory cell array, said row redundancy circuit comprising:

5 an address selector for receiving two or more address bits designating said defective cell and for selecting one of said two or more address bits;

10 a fuse box for receiving all bits of an address and storing the information of all address bits other than the one address bit selected at said address selector; and

at least one redundant decoder for decoding the output signals of said address selector and fuse box.

15 Preferably, said address selector receives three address bits designating said defective memory cell for selection, to thereby select one of said three bits.

20 Preferably, said address selector comprises a plurality of fuse means each connected to a respective address bit.

Preferably, all of said address bits are received by said address selector and processed by said redundant decoder in complementary pairs.

25 For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to Figures 2 to 5 of the accompanying diagrammatic drawings, in which:

Figure 2 is a block diagram of one example of a row redundancy circuit according to the present invention;

5 Figure 3 is a block diagram of an address selector according to an embodiment of the present invention;

Figure 4 is a schematic circuit diagram of a fuse box and row redundant decoder according to an embodiment of the present invention; and

10 Figure 5 is a table representing repairing rate of the inventive row redundancy circuit of Figure 2.

Referring to Figure 2, the inventive row redundancy circuit comprises an address selector 300, fuse box 100 and redundant decoders 200 and 200A.
15 The address selector 300 receives two or more address bits (in this case three bits) designating a defective cell to selectively output one among the two or more address bits. The fuse box 100 stores the information of the remaining address bits except the output bit selected at the address selector 300. The redundant decoders 200 and 200A decode the output signals of the address
20 selector 300 and fuse box 100.

The fuse box 100 receives row addresses RA0-RA7. The address selector 300 selects one of the three input row addresses RA0-RA2. As shown in Figure 2, all the addresses RA0-RA7 are applied to the fuse box
25 100, and moreover one of the addresses RA0 to RA2 is selectively input to the redundant decoders 200 and 200A, thereby increasing the repairing probability. Namely, as shown in Figure 5, two adjacent word lines have two

different bits after eight word lines and three different bits after sixteen word lines.

If the adjacent word lines have one different bit, in the address selector,
5 one of the addresses RA0, RA1 and RA2 is selectively input to the row redundant decoders 200 and 200A in response to the different bit, and the row addresses except the bit selected at the address selector are input to the fuse box, thus performing a repairing operation. If the adjacent word lines have two different bits, the different bits are always RA2 and RA3 and therefore
10 the address RA2 is selected as input to the row redundant decoders 200 and 200A, and the remaining addresses to the fuse box 100, thus performing a repair. If three or more bits are different, the fuse box 100 would cover too many cases to perform the repairing operation. Therefore, as shown in
15 Figure 5, the illustrated row redundant circuit achieves a repairing probability of at least 93% (i.e. $(15/16) \times 100\%$) even with a single redundancy set for each of the minimum array blocks.

In operation, the address selector 300 is enabled by cutting an enable fuse F (nodes A and B respectively take low and high levels), as shown in
20 Figure 3. Detecting a defective address in a chip test, four of the addresses of the address selector 300 among the addresses RA0, RA $\bar{0}$, RA1, RA $\bar{1}$, RA2, RA $\bar{2}$, and the enable fuse F are cut. Therefore one of the addresses RA0, RA1, RA2 which is not cut is applied to the row redundant decoder. In addition, a reset clock RESET determines the state of the nodes A and B.
25

Referring to Figure 4, showing the fuse box 100 and row redundant decoders 200, 200A, the fuse box 100 cuts a fuse pair RA i and RA \bar{i} which are the selected addresses in the address selector of Figure 3. The given

remaining fuses are cut according to the defective address, storing the row address of the defective cell. The outputs of the address selector 300 and the fuse box 100 are applied to the row redundant decoders 200 and 200A. A node C is pre-charged with a source voltage Vcc by means of a pre-charge
5 clock signal ϕDPX . The row redundant decoders 200 and 200A pass to the spare word line SWL1 or SWL2 a signal ϕX that is input to the word line drivers 211, 212, 211', 212', under the control of the output RFA_i and RFA_i' of the address selector 300, output information of the fuse box 100, and the row redundant decoder enable clock signal ϕXE . Hence, the redundancy
10 operation of the chip is readily achieved.

Although the circuits of Figures 3 and 4 are preferred embodiments of Figure 2, they may be embodied in a variety of ways. Even if the address selector 300 is made to select one of two bits, the redundancy efficiency may
15 be considerably increased compared to the prior art circuit of Figure 1. However, it should be noted that maximum efficiency is achieved by selecting from three bits.

As stated above, the illustrated circuit achieves a repairing probability
20 of at least 93% for row or word line fail even with a single redundancy set for each of the minimum array blocks, thus preventing the chip size from being increased and the yield from being reduced.

While preferred embodiments of the invention have been particularly
25 shown and described, it will be apparent to those who are skilled in the art that in the foregoing, changes in form and detail may be made without departing from the spirit and scope of the present invention.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by
5 reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except
10 combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative
15 features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

20 The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. A semiconductor memory device with a row redundancy circuit for repairing a defective cell of a memory cell array, said row redundancy circuit comprising:
 - 5 an address selector for receiving two or more address bits designating said defective cell and for selecting one of said two or more address bits;
 - 10 a fuse box for receiving all bits of an address and storing the information of all address bits other than the one address bit selected at said address selector; and
 - 15 at least one redundant decoder for decoding the output signals of said address selector and fuse box.
- 20 2. A semiconductor memory device as claimed in Claim 1, wherein said address selector receives three address bits designating said defective memory cell for selection, to thereby select one of said three bits.
3. A semiconductor memory device as claimed in Claim 1 or 2, wherein said address selector comprises a plurality of fuse means each connected to a respective address bit.
- 25 4. A semiconductor memory device according to any of the preceding claims, wherein all of said address bits are received by said address selector and processed by said redundant decoder in complementary pairs.

5. A semiconductor memory device substantially as hereinbefore described with reference to Figure 2 of the accompanying drawings.

6. A semiconductor memory device substantially as hereinbefore described
5 with reference to Figures 2 to 5 of the accompanying drawings.

Relevant Technical fields

(i) UK CI (Edition --K) G4A (AEF)

Search Examiner

S J PROBERT

(ii) Int CI (Edition 5) G06F 11/20

Databases (see over)

(i) UK Patent Office

Date of Search

(ii)

2 DECEMBER 1992

Documents considered relevant following a search in respect of claims 1-6

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
A	GB 2130770 A (WESTERN ELECTRIC) See abstract	1



Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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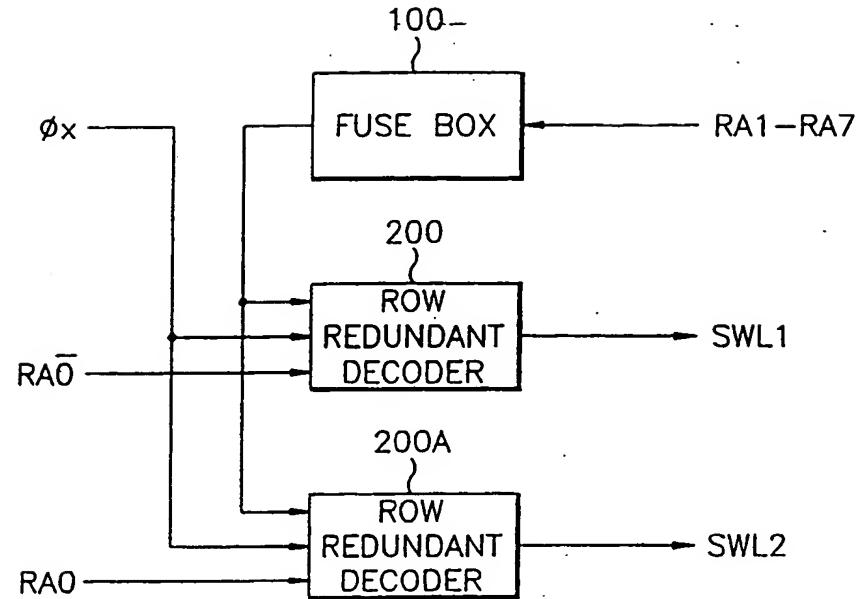
A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

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(PRIOR ART)

FIG. 1

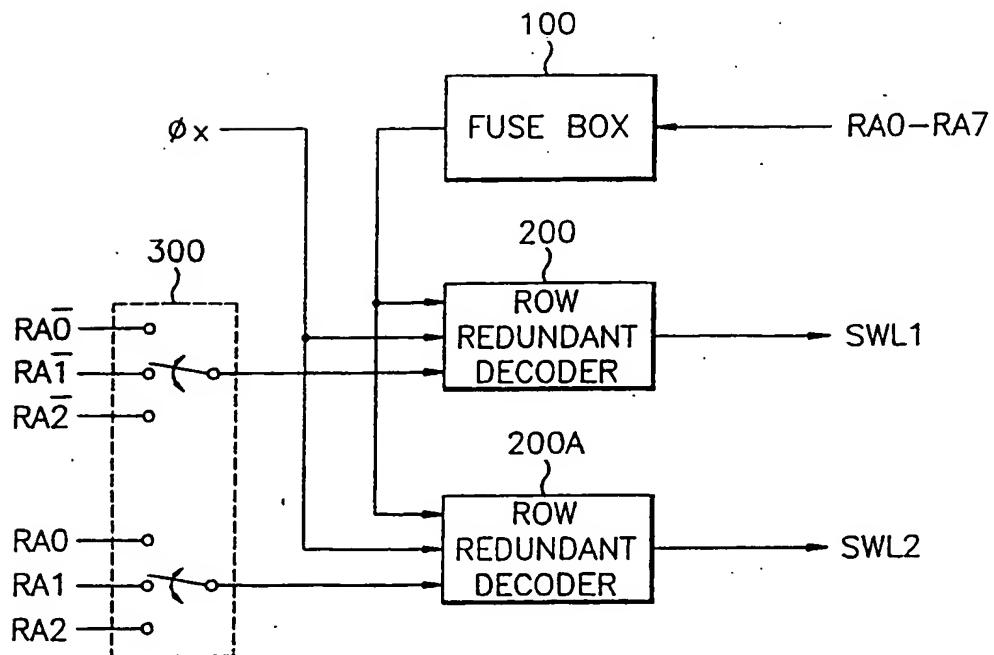


FIG. 2

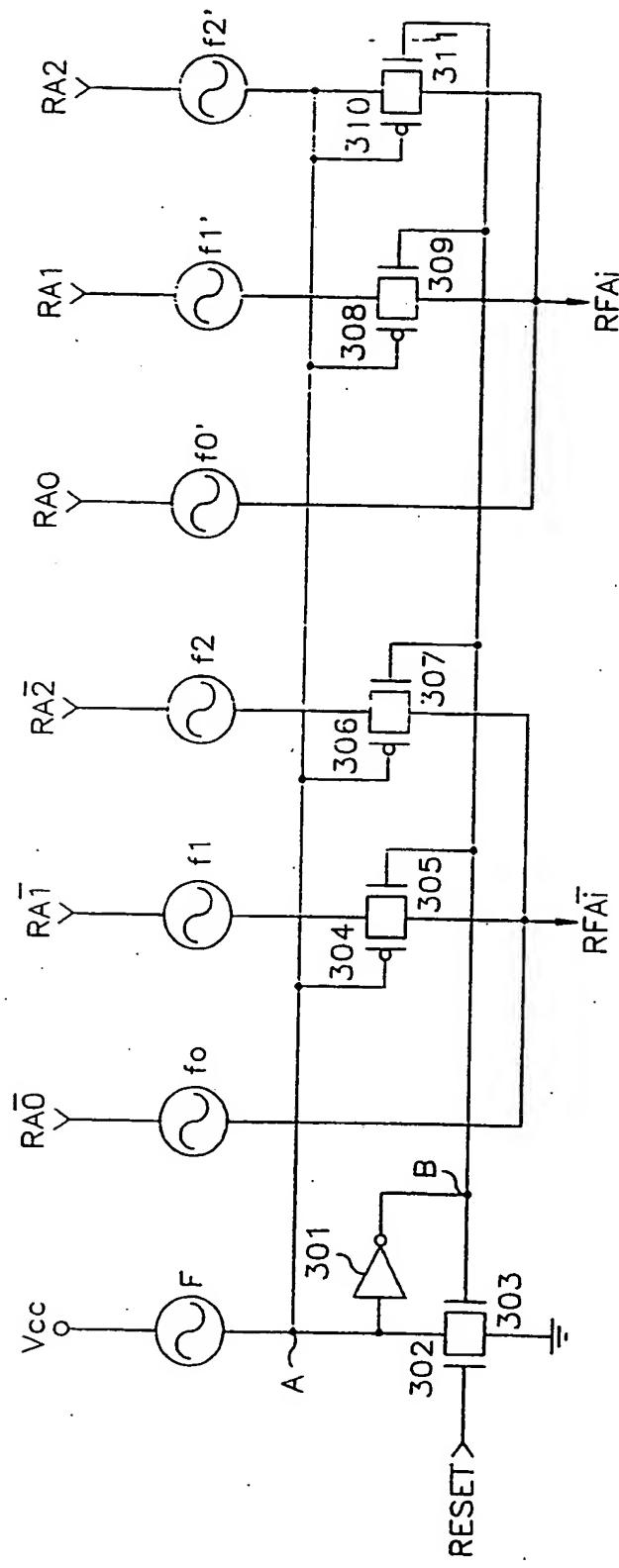


FIG. 3

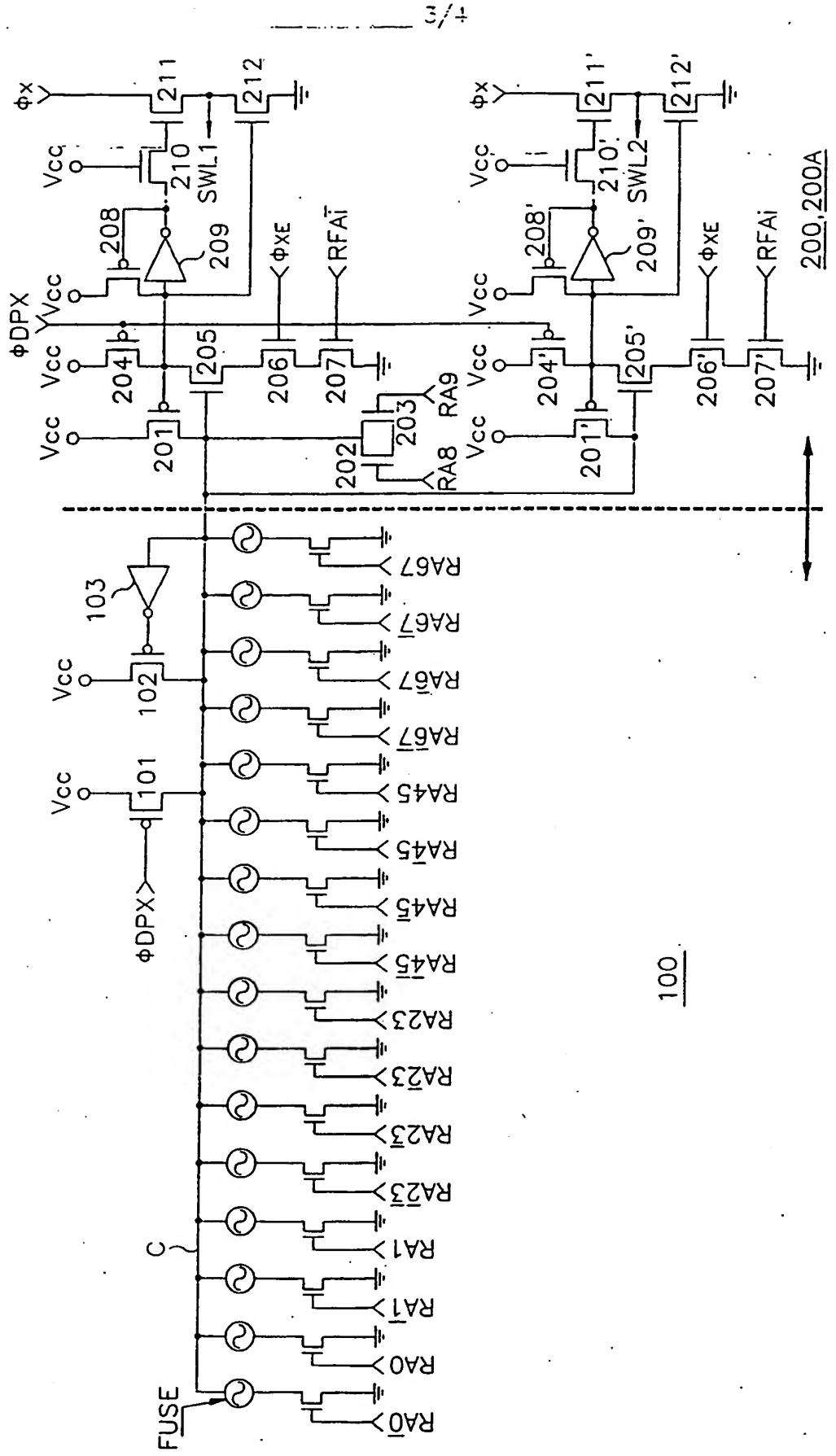


FIG. 4

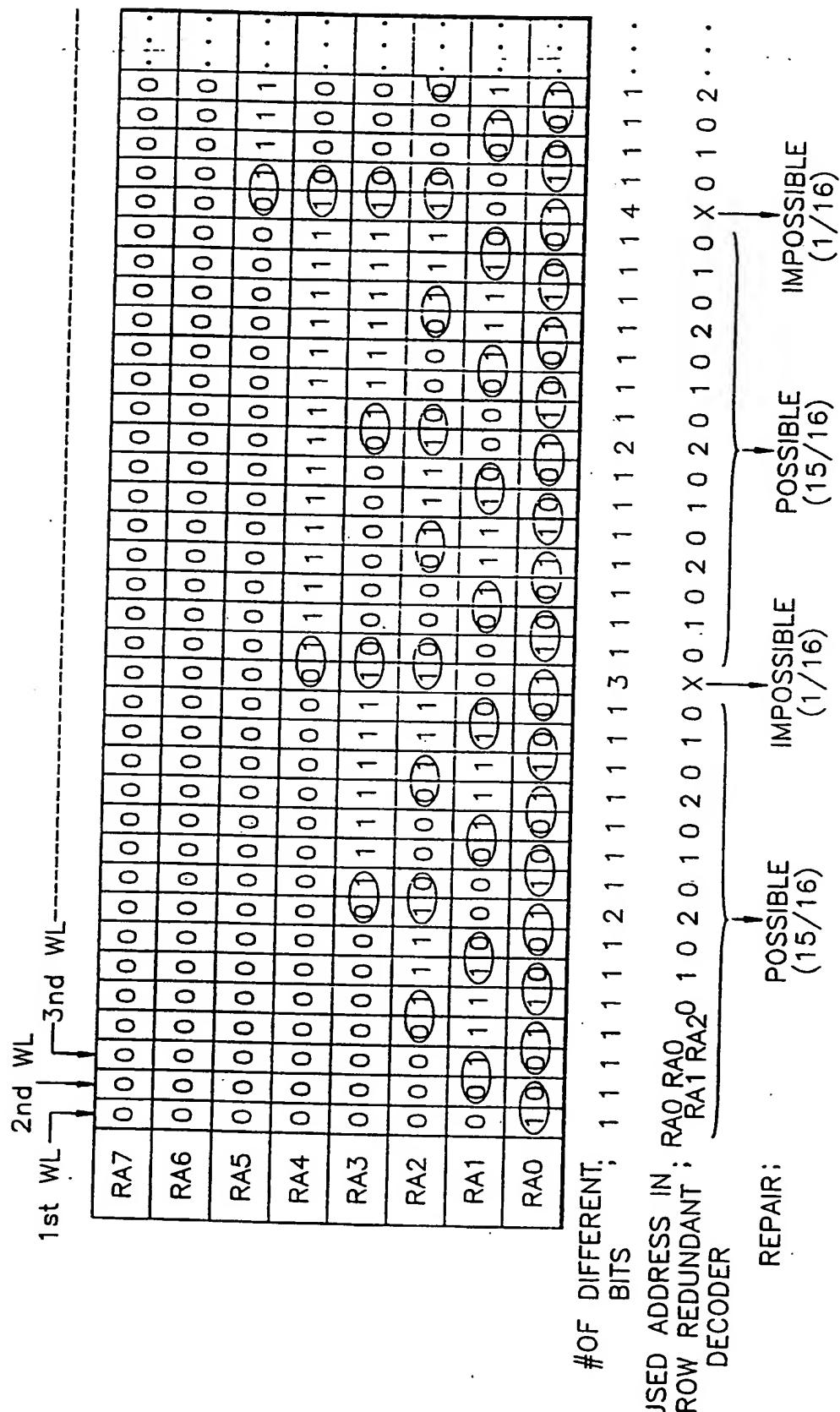


FIG. 5.

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